

EXHIBIT 13

Thursday, January 12, 2006

SHEET 1

1

1 IN THE UNITED STATES DISTRICT COURT
2 IN AND FOR THE DISTRICT OF DELAWARE

3 - - -
4 AMPEX CORPORATION, : CIVIL ACTION
5 Plaintiff, :
6 v :
7 EASTMAN KODAK COMPANY, :
8 ALTEK CORPORATION, and :
9 CHINON INDUSTRIES, INC., :
Defendants. : NO. 04-1373 (KAJ)

10 - - -
11 Wilmington, Delaware
12 Thursday, January 12, 2006 at 9:30 a.m.
13 TUTORIAL CONFERENCE

14 - - -
15 BEFORE: HONORABLE KENT A. JORDAN, U.S.D.C.J.

16 - - -
17 APPEARANCES:

18 MORRIS NICHOLS ARSHT & TUNNELL
19 BY: JULIA HEANEY, ESQ.

20 and

21 ROPES & GRAY, LLP
22 BY: NORMAN H. BEAMER, ESQ.
23 (Palo Alto, California)

24 and

25 Brian P. Gaffigan
Registered Merit Reporter

Thursday, January 12, 2006

<p>SHEET 2</p> <p>2</p> <p>1 APPEARANCES: (Continued)</p> <p>2</p> <p>3 ROPES & GRAY, LLP.</p> <p>4 BY: JESSE J. JENNER, ESQ.</p> <p>5 (New York, New York)</p> <p>6 Counsel for Plaintiff</p> <p>7 PRICKETT JONES & ELLIOTT, P.A.</p> <p>8 BY: PAUL M. LUKOFF, ESQ., and</p> <p>9 DAVID E. BRAND, ESQ.</p> <p>10 and</p> <p>11 WILMER CUTLER PICKERING HALE and DORR, LLP</p> <p>12 BY: DONALD R. STEINBERG, ESQ.,</p> <p>13 MICHAEL J. SUMMERSGILL, ESQ., and</p> <p>14 SARAH E. WHITMAN, ESQ.</p> <p>15 (Boston, Massachusetts)</p> <p>16 Counsel for Defendants</p> <p>17 - oOo -</p> <p>18 PROCEEDINGS</p> <p>19 (REPORTER'S NOTE: The following tutorial</p> <p>20 conference was held in open court, beginning at 9:30 a.m.)</p> <p>21 THE COURT: Good morning. Please be seated.</p> <p>22 Why don't we go ahead and we'll start with some</p> <p>23 introductions.</p> <p>24 MS. HEANEY: Good morning, Your Honor. Julie</p> <p>25 Heaney for plaintiff Ampex Corporation. We have Norman</p> <p>Beamer from Robes & Gray and Jessie Jenner who represent</p> <p>Ampex.</p>	<p>4</p> <p>1 (Documents passed forward.)</p> <p>2 THE COURT: Thank you.</p> <p>3 MR. BEAMER: Good morning, Your Honor. I'm</p> <p>4 Norman Beamer representing Apex, and I have a tutorial</p> <p>5 presentation. First, we're going to discuss the</p> <p>6 patent-in-suit, which is the '121 patent issued to Ampex.</p> <p>7 It's entitled, Electronic Still Store With High Speed</p> <p>8 Sorting and Method of Operation, issued in 1989, applied</p> <p>9 for in 1983.</p> <p>10 A still store is basically a device which holds</p> <p>11 in digital form still images. And the invention is directed</p> <p>12 to the idea of sorting and retrieving images rapidly.</p> <p>13 The invention originally arose out of a</p> <p>14 development of a product that Ampex called the ESS-3. ESS</p> <p>15 stands for electronic still store. It was first introduced</p> <p>16 at the NAB Convention in 1983 in Las Vegas. And this is a</p> <p>17 picture of the original ESS-3 as demonstrated on the floor</p> <p>18 of the convention. As you can see, it contains a user</p> <p>19 console, various electronics and a magnetic disk storage</p> <p>20 similar to what kind of disk storage you have in an ordinary</p> <p>21 personal computer.</p> <p>22 This is an early brochure of the ESS-3, again</p> <p>23 showing the various components. In 1983, of course,</p> <p>24 electronics were not as compact as they are today, and so</p> <p>25 the electronics were in two different chassis.</p>
<p>3</p> <p>1 MR. JENNER: Good morning, Your Honor.</p> <p>2 THE COURT: All right. Who is going to be</p> <p>3 making the presentation today?</p> <p>4 MR. BEAMER: I am, Your Honor. Norman Beamer.</p> <p>5 THE COURT: All right.</p> <p>6 MR. LUKOFF: And Paul Lukoff on behalf of the</p> <p>7 defendants Kodak, et al. And with me today are Michael</p> <p>8 Summersgill and David Steinberg from the Wilmer Cutler</p> <p>9 Pickering Hale and Dorr firm. They'll both be making</p> <p>10 partial presentations on the defense part.</p> <p>11 THE COURT: All right. Can I have the names</p> <p>12 again, please?</p> <p>13 MR. LUKOFF: I'm sorry?</p> <p>14 THE COURT: The names one more time?</p> <p>15 MR. LUKOFF: Michael Summersgill.</p> <p>16 MR. STEINBERG: And Donald Steinberg.</p> <p>17 THE COURT: All right. Thank you very much.</p> <p>18 Go ahead. I'll give the floor to you, Mr. Beamer, to start</p> <p>19 with.</p> <p>20 MR. BEAMER: Thank you, Your Honor. I have a</p> <p>21 book that contains still versions of some of the pictures</p> <p>22 that I am going to be using. If I may hand up a copy for</p> <p>23 Your Honor?</p> <p>24 THE COURT: Please do.</p> <p>25 MR. BEAMER: And an extra copy.</p>	<p>5</p> <p>1 THE COURT: Let me ask you a question, if I</p> <p>2 might.</p> <p>3 MR. BEAMER: Sure.</p> <p>4 THE COURT: In, throughout the patent, it</p> <p>5 talks about still store, uses it as a term of art. Can</p> <p>6 you explain just that term to start with more completely</p> <p>7 for me?</p> <p>8 MR. BEAMER: Sure. Well, a still store simply</p> <p>9 refers to a device which can store still images. In the</p> <p>10 context of television broadcasting, a still store was a</p> <p>11 device such as we see here used to rapidly retrieve digital</p> <p>12 versions of still images for the purpose of displaying them</p> <p>13 in a TV broadcast. For example, in a news show, obviously</p> <p>14 there is a series of still images that are displayed while</p> <p>15 the newscaster is giving, was reading off the news. And so</p> <p>16 that this is just a way of rapidly retrieving still images</p> <p>17 in a television broadcast situation. But a still store, at</p> <p>18 least Ampex would say that a still store simply means what</p> <p>19 it says: a storage of still, a device which stores still</p> <p>20 images.</p> <p>21 THE COURT: Okay. Thank you.</p> <p>22 MR. BEAMER: Here is a snippet of a promotional</p> <p>23 video for the ESS-3 which gives kind of an overview.</p> <p>24 (AUDIO SOUND): ESS-3 system. A picture from</p> <p>25 any standard composite video source, camera, film chain,</p>

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<p>SHEET 3</p> <p style="text-align: right;">6</p> <p>1 line, character generator or VTR is captured and digitally 2 stored on a standard computer-style disk drive. One drive 3 can store and access as many as 400 stills. Up to 16 drives 4 may be included in the system, thus making available as many 5 as 6400 online images, each identified by number and 6 available for recall in less than a second.</p> <p>7 For visual identification, or for browsing, 8 reduced-size images with ident numbers are presented 16 at 9 a time, allowing a quick and positive review of an entire 10 online library.</p> <p>11 MR. BEAMER: So that feature that is shown in 12 the last portion of the video, the browse screen, is what 13 the invention is all about. Here is another picture of the 14 browse screen in the brochure. And that was a feature 15 touted by Ampex, and that's the feature that is described 16 and claimed in the patent.</p> <p>17 Basically, the idea is you have all these 18 images stored on some type of bulk storage medium such as a 19 magnetic drive and you want to be able to browse through and 20 choose the particular still that you want to retrieve. And 21 it's convenient to do so using this kind of a browse screen 22 where multiple reduced-size pictures are displayed on the 23 screen all at once. You quickly browse through them, pick 24 the one that you want and select that as your full-sized 25 picture to be displayed.</p>	<p style="text-align: right;">8</p> <p>1 We have an animated version of this image to 2 show the operation of the invention. And I have expanded 3 out some of the boxes and filled in some of the boxes with 4 examples from the real world. For the input, we're using 5 an ordinary TV camera. It's pointed at a moving image. 6 And that moving image is stored in digital form in the 7 frame store. This is just a representation of that. It's 8 actually digital 1s and 0s. The contents of that frame 9 store is read out through the output circuitry and 10 displayed on a monitor.</p> <p>11 Now, when the user wants to capture an image, he 12 indicates with the appropriate command the images captured. 13 And I'll describe what is happening. I'll run this again 14 and describe what is happening.</p> <p>15 The picture is in the frame store. It's frozen. 16 It's sent to the size reducer and reduced. The reduced size 17 version is placed in the frame store and then both are 18 stored in disk store. I'll do that once more.</p> <p>19 The image is captured. It's reduced. The 20 reduced version is stored in frame store and then both are 21 stored in disk store.</p> <p>22 Now, let's assume that the user has captured 23 a number of images and now has a library of stills. You 24 will see that for every still full-sized image, there is a 25 corresponding reduced size image. Now, let's assume that</p>
<p style="text-align: right;">7</p> <p>1 So how does the patent do that? 2 Well, there is one figure, as you I'm sure have 3 noticed in the patent, a block diagram. First, there is a 4 video input which is -- could be, as that video showed, 5 could be a TV camera or another still store or a character 6 generator, any sort of source of images. That image is 7 normally in analog form. The real world is analog, i.e., 8 things vary continuously. For this, this invention takes 9 that analog image and converts it to digital form using an 10 input analog-to-digital converter. It then stores that 11 digital information in a frame store. A frame store is 12 simply a random access memory or RAM, such as -- again, 13 such as the RAM that is in a personal computer.</p> <p>14 The contents of that frame store can be then 15 displayed on a monitor, but first it has to be converted 16 back into analog by the output digital-analog converter and 17 further processed so as to be displayed on a monitor.</p> <p>18 When you want to capture an image, you move it 19 into the frame stored in accord with the invention, you 20 reduce the size of the image in a size reducer, and then 21 you store both the full-sized and reduced-size image into 22 a disk store or other bulk storage medium.</p> <p>23 A CPU, central processing unit, i.e., a 24 microprocessor, controls the whole operation of the system; 25 and then there is a user console to allow user input.</p>	<p style="text-align: right;">9</p> <p>1 some time later, the user wants to retrieve an image. 2 Well, he can retrieve any full-sized image by pressing the 3 appropriate command; and here we're just simulating that. 4 But suppose he wants to browse the images. He pushes the 5 appropriate command and what happens are the prestored 6 reduced-size images are retrieved and placed into the frame 7 store at the appropriate position so as to display this 8 matrix of reduced-size images.</p> <p>9 I'll do that again. You will see that 10 whether -- that is why the invention teaches to store the 11 reduced-size images, for his rapid retrieval and generation 12 of the browse screen.</p> <p>13 So now the user can select one of those 14 reduced-size images and fetch the corresponding full-sized 15 image rapidly.</p> <p>16 Let me show you how that works in a contemporary 17 device. We have here one of the Kodak cameras. It's 18 warming up. And so just as the TV camera in the example, 19 this is like a small TV camera that can be pointed anywhere. 20 And I can take an image and I am now freezing the image, 21 capturing it and it's now being stored on to the bulk 22 storage device, which in this case is a memory card, and it 23 turns out that a reduced-size image is stored along with 24 that full-sized image.</p> <p>25 I'll take another picture. These are not very</p>

EXHIBIT 14

CONFIDENTIAL EXHIBIT

EXHIBIT 15

CONFIDENTIAL EXHIBIT

EXHIBIT 16

CONFIDENTIAL EXHIBIT

EXHIBIT 17

CONFIDENTIAL EXHIBIT

EXHIBIT 18



HY57V561620C(L)T(P)

4 Banks x 4M x 16Bit Synchronous DRAM

DESCRIPTION

The HY57V561620C(L)T(P) Series is a 268,435,456bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V561620C(L)T(P) Series is organized as 4banks of 4,194,304x16.

HY57V561620C(L)T(P) Series is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule.)

FEATURES

- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch (Leaded Package or Lead Free Package)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM, LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 8192 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8 or Full page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable CAS Latency ; 2, 3 Clocks

ORDERING INFORMATION

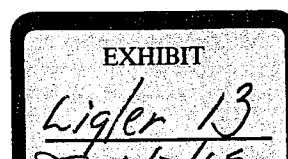
Part No.	Clock Frequency	Power	Organization	Interface	400mil 54pin TSOP-II
HY57V561620C(L)T(P)-6	166MHz	(Normal) / Low Power	4Banks x 4Mbits x16	LVTTTL	(Leaded) / Lead Free
HY57V561620C(L)T(P)-7	143MHz				
HY57V561620C(L)T(P)-K	133MHz				
HY57V561620C(L)T(P)-H	133MHz				
HY57V561620C(L)T(P)-8	125MHz				
HY57V561620C(L)T(P)-P	100MHz				
HY57V561620C(L)T(P)-S	100MHz				

Note :

1. HY57V561620CT Series : Normal power & Leaded 54Pin TSOP II
2. HY57V561620CLT Series : Low power & Leaded 54Pin TSOP II
3. HY57V561620CTP Series : Normal power & Lead Free 54Pin TSOP II
4. HY57V561620CLTP Series : Low power & Lead Free 54Pin TSOP II

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Rev. 0.5 / June 2004

AX200163

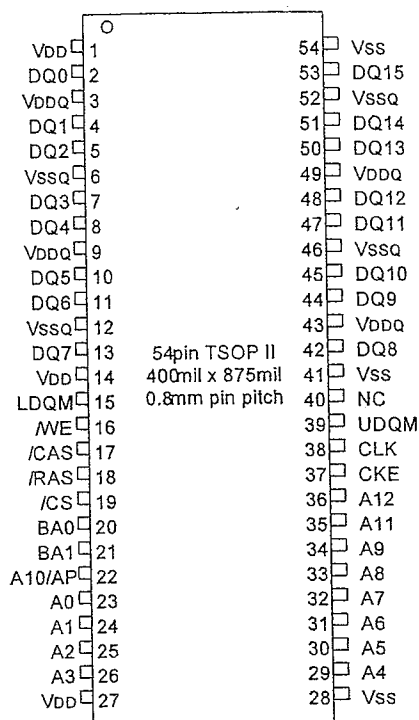


AX200163



HY57V561620C(L)T(P)

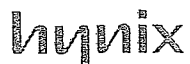
PIN CONFIGURATION



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
CS	Chip Select	Enables or disables all inputs except CLK, CKE, UDQM and LDQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{\text{RAS}}$ activity Selects bank to be read/written during CAS activity
A0 ~ A12	Address	Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA8 Auto-precharge flag : A10
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation Refer function truth table for details
UDQM, LDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

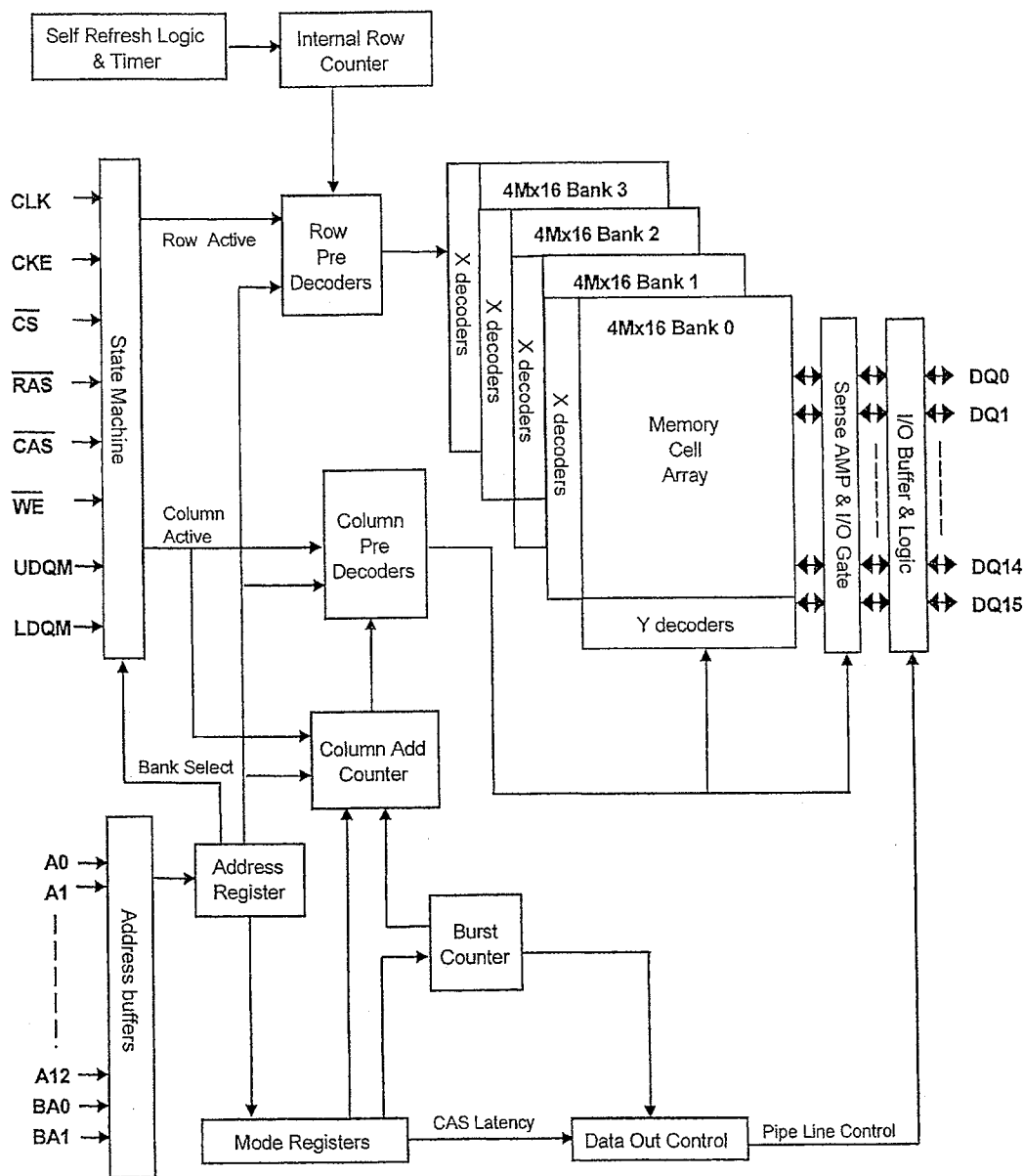
AX200164



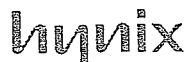
HY57V561620C(L)T(P)

FUNCTIONAL BLOCK DIAGRAM

4Mbit x 4banks x 16 I/O Synchronous DRAM



AX200165



HY57V561620C(L)T(P)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature - Time	TSOLDER	260 - 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low Voltage	VIL	- 0.3	0	0.8	V	1,3

Note :

1. All voltages are referenced to VSS = 0V
2. VIH (max) is acceptable 5.6V AC pulse width with ≤3ns of duration
3. VIL (min) is acceptable -2.0V AC pulse width with ≤3ns of duration

AC OPERATING CONDITION (TA=0 to 70°C, VDD=3.3 ± 0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :

1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)
For details, refer to AC/DC output circuit

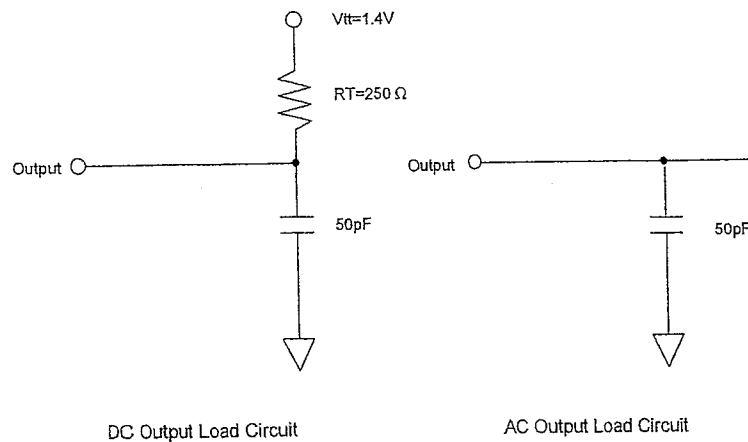


HY57V561620C(L)T(P)

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-6T/K/H		-8P/S		Unit
			Min	Max	Min	Max	
Input capacitance	CLK	Cl1	2.5	3.5	2.5	4.0	pF
	A0 ~ A12, BA0, BA1, CKE, CS, RAS, CAS, WE, UDQM, LDQM	Cl2	2.5	3.8	2.5	5.0	pF
Data input / output capacitance	DQ0 ~ DQ15	Cl/O	4.0	6.5	4.0	6.5	pF

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, VDD=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note :

1. VIN = 0 to 3.6V, All other pins are not tested under VIN = 0V
2. DOUT is disabled, VOUT = 0 to 3.6V



HY57V561620C(L)T(P)

DC CHARACTERISTICS II (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Test Condition	Speed							Unit	Note
			-6	-7	-K	-H	-8	-P	-S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	130	110	110	110	100	100	100	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	2							mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	1								
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), CS ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V	20							mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	10								
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	3							mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	3								
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), CS ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V	30							mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	25								
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	150	130	130	130	130	110	110	mA	1
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active	220	220	220	220	200	200	200	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	3							mA	3
			1.5							mA	4

Note :

- 1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
- 2.Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
- 3.HY57V561620CT(P)-6/7/K/H/8/P/S
- 4.HY57V561620CLT(P)-6/7/K/H/8/P/S



HY57V561620C(L)T(P)

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-7		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency = 3	tCK3	6		7		7.5		7.5		8		10		10		ns	
	CAS Latency = 2	tCK2	7.5	1000	10	1000	7.5	1000	10	1000	10	1000	10	1000	12	1000	ns	
Clock High Pulse Width		tCHW	2.5	-	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Access Time From Clock	CAS Latency = 3	tAC3	-	5.4	-	5.4	-	5.4	-	5.4	-	6	-	6	-	6	ns	2
	CAS Latency = 2	tAC2	-	6	-	6	-	5.4	-	6	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	2.7	-	2.7	-	2.7	-	2.7	-	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	1	-	1	-	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z Time	CAS Latency = 3	tOHZ3	2.7	5.4	2.7	5.4	2.7	5.4	2.7	5.4	3	6	3	6	3	6	ns	
	CAS Latency = 2	tOHZ2	2.7	5.4	2.7	5.4	2.7	5.4	3	6	3	6	3	6	3	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns

2.Access times to be measured with input signals of 1v/ns edge rate



HY57V561620C(L)T(P)

AC CHARACTERISTICS II

Parameter		Symbol	-6		-7		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RAS Cycle Time	Operation	IRC	60	-	60	-	60	-	65	-	68	-	70	-	70	-	ns	
	Auto Refresh	IRRC	60	-	60	-	60	-	65	-	68	-	70	-	70	-	ns	
RAS to CAS Delay		IRCD	18	-	18	-	15	-	20	-	20	-	20	-	20	-	ns	
RAS Active Time		IRAS	42	100K	42	100K	45	100K	45	100K	48	100K	50	100K	50	100K	ns	
RAS Precharge Time		IRP	18	-	18	-	15	-	20	-	20	-	20	-	20	-	ns	
RAS to RAS Bank Active Delay		IRRD	12	-	14	-	15	-	15	-	16	-	20	-	20	-	ns	
CAS to CAS Delay		ICCD	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		IWTL	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Write Recovery Time		IWR	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Data-In to Active Command		IDAL	5	-	5	-	5	-	5	-	5	-	5	-	5	-	CLK	
DQM to Data-Out Hi-Z		IDQZ	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		IDQM	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		IMRD	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	CAS Latency = 3	IPOZ3	3	-	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
	CAS Latency = 2	IPOZ2	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		IPDE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		ISRE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		IREF	-	64	-	64	-	64	-	64	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

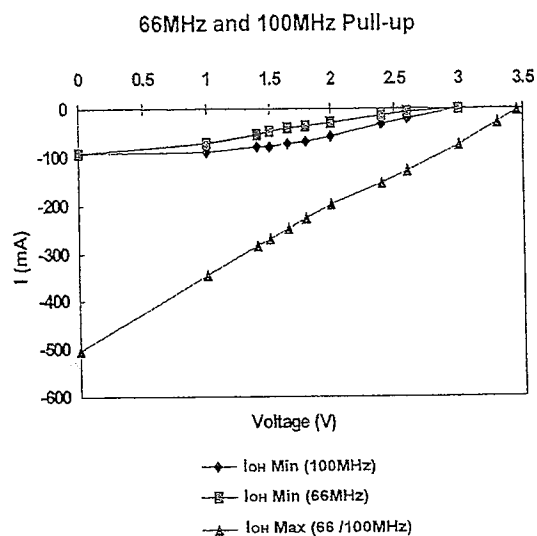


HY57V561620C(L)T(P)

IBIS SPECIFICATION

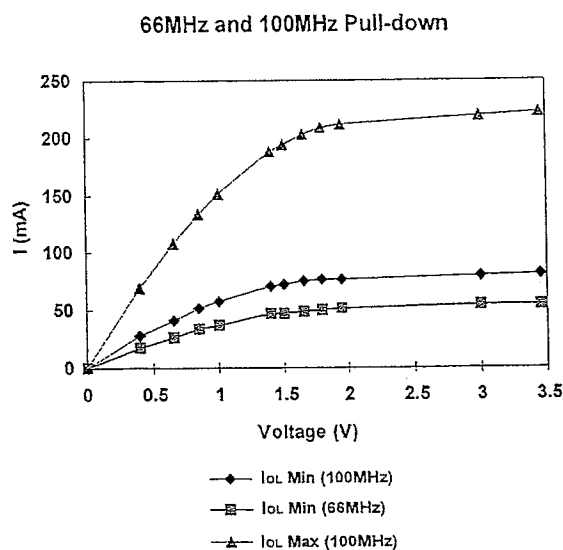
IOH Characteristics (Pull-up)

Voltage	100MHz (Min)	100MHz (Max)	66MHz (Min)
(V)	I(mA)	I(mA)	I(mA)
3.45		-2.4	
3.3		-27.3	
3.0	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73	-248	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0	-93	-502.4	-93



IOL Characteristics (Pull-down)

Voltage	100MHz (Min)	100MHz (Max)	66MHz (Min)
(V)	I(mA)	I(mA)	I(mA)
0	0	0	0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9



AX200171



HY57V561620C(L)T(P)

DEVICE OPERATING OPTION TABLE

HY57V561620C(L)T(P)-6

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
133MHz(7.5ns)	2CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns

HY57V561620C(L)T(P)-7

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
133MHz(7.5ns)	2CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns

HY57V561620C(L)T(P)-K

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	2CLKs	2CLKs	6CLKs	8CLKs	2CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY57V561620C(L)T(P)-H

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY57V561620C(L)T-8

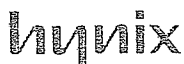
	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HY57V561620C(L)T(P)-P

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HY57V561620C(L)T(P)-S

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns



HY57V561620C(L)T(P)

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DQM	ADDR	A10/ AP	BA	Note			
Mode Register Set		H	X	L	L	L	L	X	OP code						
No Operation		H	X	H	X	X	X	X	X						
				L	H	H	H								
Bank Active		H	X	L	L	H	H	X	RA		V				
Read		H	X	L	H	L	H	X	CA	L	V				
Read with Autoprecharge										H					
Write		H	X	L	H	L	L	X	CA	L	V				
Write with Autoprecharge										H					
Precharge All Banks		H	X	L	L	H	L	X	X	H	X				
Precharge selected Bank										L	V				
Burst Stop		H	X	L	H	H	L	X	X						
DQM		H	X					V	X						
Auto Refresh		H	H	L	L	L	H	X	X						
Burst-Read-Single-WRITE		H	X	L	L	L	H	X	A9 Pin High (Other Pins OP code)						
Self Refresh ¹	Entry	H	L	L	L	L	H	X	X						
	Exit	L	H	H	X	X	X	X							
Precharge power down	Entry	H	L	H	X	X	X	X	X						
				L	H	H	H								
	Exit	L	H	H	X	X	X	X							
				L	H	H	H								
Clock Suspend	Entry	H	L	H	X	X	X	X	X						
				L	V	V	V								
	Exit	L	H	X				X							

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA = Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation



HY57V561620C(L)T(P)

PACKAGE INFORMATION

400mil 54pin Thin Small Outline Package

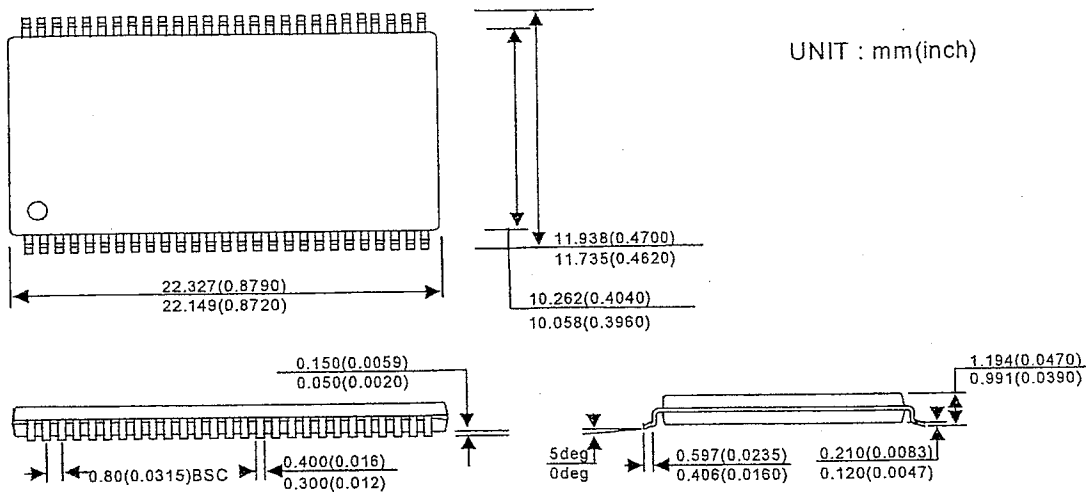


EXHIBIT 19

CONFIDENTIAL EXHIBIT

EXHIBIT 20

CONFIDENTIAL EXHIBIT

EXHIBIT 21

CONFIDENTIAL EXHIBIT

EXHIBIT 22

CONFIDENTIAL EXHIBIT

EXHIBIT 23

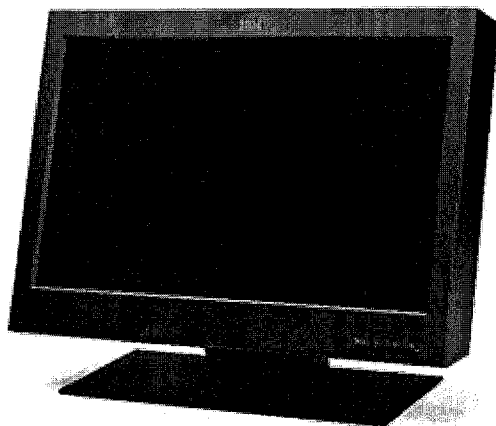


T221 22.2-inch QUXGA TFT Flat Panel Monitor (9503) - Overview

✦ Applicable countries and regions

Document options

Printable version



IBM & Lenovo



ThinkPad,
ThinkCentre and
other PC products are
now products of
Lenovo.

lenovo
Support & downloads

- Service parts
- Files (For Matrox video card included w/monitor)
- Files (For FireGL Digital video card, not included w/monitor)
- NVIDIA drivers file for Microsoft XP and Windows 2000
- NVIDIA Quadro FX 1100 BIOS Update
- Files - Firmware Utility Update
- Files - Firmware utility Foundation Model
- Files - Resolution switching utility by Hot Key software update
- Files - Color Management software utility
- Files - Configuration files for Linux environment
- Publications

At a glance

With the new T221 flat-panel monitor, you can view business-critical applications with an astounding level of clarity. Features include:

- 22.2-inch viewable image area
- 3840 x 2400 addressability (QUXGA-W)
- 9.2 million total pixels, 204 pixel density per inch (80 per cm)
- 16.7 million colors, 8-bit drivers
- Tilt stand
- Detachable Video Electronics Standards Association (VESA) standard mount size (100 mm) stand
- Available in Business Black

Warranty

United States, Canada, Latin America, Europe, Middle East, and Africa
3 year Limited - customer carry-in exchange

Asia Pacific (Japan only)

1 year Limited -customer carry-in exchange

Packaging

You will receive one box containing the following items:

- Monitor
- Attached tilt stand
- Detached external power supply (ac adapters)
- Power cord
- Corresponding cable and card
 - 9503-DG1: Matrox cables(x2) with G200MMS card
 - 9503-DG3: DVI cable(x1)
- User's Guide
- Japanese warranty card (Japan only)

Product dates

Worldwide

- Announce date: 9 Oct 2001
- Planned availability date: October 2001

Technical specifications

Physical, environmental, and compatibility specifications as known at time of announcement

Weight

- 26.4 lbs
- 12 kg

Height

- 17.2 inches
- 437 mm

Width

- 21.5 inches
- 547 mm

Depth

- 7.7 inches
- 196 mm

Power requirements

- Input voltage: 100 to 240 V ac
- Frequency: 50/60 Hz
- Power consumption (Maximum): 150 watts
- Power consumption (Normal Use): <135 watts typical
- Power consumption (VESA Standby): 15 watts maximum
- Power consumption (VESA Suspend): 15 watts maximum
- Power consumption (VESA Off): 15 watts maximum

NOTE: Actual power consumption depends on the screen mode used, the images displayed, and how user controls are set.

Altitude

- Operating: 0 to 12,000 ft

- Shipping: 0 to 40,000 ft
- Storage: 0 to 12,000ft

Operating

- Temperature: 0 to 35degrees celsius
- Relative humidity: 8% to 80%
- Altitude: 0 to 12,000ft

Storage

- Temperature: -20 to 60degrees celsius
- Relative humidity: 5% to 95%
- Altitude: 0 to 12,000ft

Shipping

- Temperature: -20 to 60degrees celsius
- Relative humidity: 5% to 95%
- Altitude: 0 to 40,000ft

Regulatory agency approvals

Safety

- UL (U.S.)
- CSA (Canada)
- IEC950 CB Report
- CE Mark (Europe)

EMC

- FCC Class A (U.S.)
- CE Mark (Europe)
- VCCI Class Class A (Japan)
- CISPR22 A
- AN/NZS 3548

Software requirements

The T221 color monitor supports the following display modes:

Resolution	Refresh Rate
640 x 480	60 Hz
640 x 480	72 Hz
640 x 480	75 Hz
640 x 480	85 Hz
800 x 600	56 Hz
800 x 600	60 Hz
800 x 600	72 Hz
800 x 600	75 Hz
800 x 600	85 Hz
1024 x 768	60 Hz
1024 x 768	70 Hz
1024 x 768	75 Hz
1024 x 768	85 Hz

1280 x 1024	60 Hz
1280 x 1024	75 Hz
1600 x 1200	60 Hz
3840 x 2400	41 Hz, stripe mode

NOTE: (3840 x 2400 41 Hz, tile mode, will be supported by the end of Oct 2001)

Appropriate video-adaptor hardware and software must be installed in the attaching system unit.

Supported operating systems

- Microsoft Windows 2000
- Linux-2.2x Kernels*

* FireGL4 card support only and will be available at the end of October.

Compatibility

Supported display modes are a function of the attaching system unit. The full range of display modes available with these monitors may not be available or supported with all combinations of system units, their operating systems, and application software.

Limitations

- The number of colors shown in any display mode (up to a maximum of 16.7 million) is not limited by the monitor, but depends on the capabilities of the video adapter in the system unit.
- Certain functions require the system unit to be similarly configured, so all monitor functions may not be enabled when attached to a particular system unit.
- The 22.2-inch TFT monitor has nearly 28 million subpixel transistors laid over an area exceeding 220 square inches. There may be a small number of these sub-pixels which are missing, discolored, or always lit. This an intrinsic characteristic of TFT manufacturing. The T221 monitor may have up to 20 defective sub-pixels.

Applicable countries and regions

Worldwide

[⬆ Back to top](#)

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Last modified: 2004-11-22

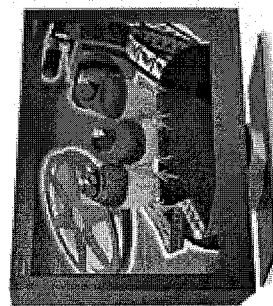
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 [Printable version](#)

EXHIBIT 24



VP2290b



Widescreen VP2290b LCD, the professional's choice.

ViewSonic's VP2290b widescreen 22.2" digital LCD raises image precision to a new level with revolutionary 27.6 million-dot (RGB sub-pixel) imagery with awe-inspiring, depth and clarity. An ultra-high 9.2 **MEGAPIXEL**


RESOLUTION OFFERS EXTRAORDINARY

DETAIL, ideal for satellite imaging and digital content creation. New AGS-1 anti-glare coating eliminates glare in almost any lighting situation for rich, saturated color.

The purely digital interface produces artifact-free, **PHOTO-REALISTIC IMAGES** with vivid TV-like, HD-compliant colors for video rendering, film restoration and graphic arts. A powerful complement to today's high-end PCs, Macs, Sun and SGI workstation, choose the VP2290b for the ultimate in LCD performance.

View a complete list of **applications and industries and compatible video cards.**

Download **drivers and utilities** for the VP2290b.


Case color: 



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Product Details

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- [Accessories](#)
- [Awards](#)
- [User Guide](#)

 [PDF Product Comparison Chart \(413 K\)](#)

 [PDF Specsheet \(292 K\)](#)
[Download Drivers/Utilities](#)

- [Press Releases](#)
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Features

9.2 mega pixel (27.6 million RGB dots)

Ultra-high 204 pixel per inch (PPI) produces stunning picture clarity and photo-like images.

Widescreen 16:10 aspect ratio

Widescreen format allows desktop publishing professionals to display two full pages of text and graphics simultaneously.

5X pixel density LCD display

Advanced high-resolution liquid crystal panel technology boosts pixel density up to five times higher than a normal LCD display for superior picture clarity and perfect focus.

Pure digital interface

Digital interface ensures original data integrity for spectacular, crystal-clear images.

Broad, accurate color gamut

conforms to ITU 709 HDTV color standard accurately reproducing true, vibrant colors.

Powerfully compatible

Compatible with PCs, Macs, Sun and SGI workstations.

Full 22.2" viewable screen

3840x2400 optimum resolution

High brightness and contrast

235-nit (typ) brightness and 400:1 (typ) contrast ratio for rich, detailed images.

Advanced AGS-1 anti-glare coating

Eliminates glare under almost any ambient lighting.

XtremeView? performance

Up to 170° viewing angles horizontally and 170° vertically, providing image clarity from all directions.

Liquid View? Software included free

Enlarge desktop icons, fonts and toolbars? even MS application toolbars? up to 200% for easy legibility.

Three-year limited warranty

24/7 free technical and customer support*.



Specifications

LCD Panel	Type	22.2" Color TFT active matrix QUXGA-W LCD
	Display Area	18.8" (horizontal) x 11.7" (vertical); 22.2" diagonal
	Optimum Resolution	3840x2400
	Contrast Ratio	400:1 (typ)
	Viewing Angle	170° horizontal, 170° vertical @ CR>10
	Brightness	235 cd/m2 (typ)
	Aspect Ratio	Native 16:9.6 or Multiple ratio depending on mode setting
	Color Depth	8-bits/color (16.7 million)
	Surface	AGS-1 anti-glare coating
	Digital Frequency	4 TMDS digital interface
VIDEO INPUT	Pixel Frequency	fh: 31~105kHz; fv: 50~85Hz
	Pixel Frequency	165 MHz/link
	PC	VGA (x5 expanded), SVGA (x4 expanded), XGA (x3 expanded), SXGA (x2 expanded), UXGA (x2 expanded), UXGA-Wide (x2 expanded), 2K x 1.5K, and QUXGA-Wide (native)
COMPATIBILITY	Mac?	Power Mac? G3/G4
	Workstations	Sun, SGI
	Digital	TMDS DVI-D
CONNECTOR	Power	16V DC in, DC to head
	Voltage	AC 100?240V AC
	Frequency	50/60Hz
POWER	Consumption	150W (<15W in standby)
	Basic	Menu/enter, left arrow, right arrow, on/off

REGULATIONS	OnView?	Brightness, video input submenu, information submenu, exit CE Mark, CISPR22, EN 60950, FCC-A, IEC 60950, ISO 13406-2, TUV ergonomics, TUV GS, UL/CSA 60950, VCCI-A, UL2601 (VP2290b-3-med option)
DIMENSIONS (WxHxD)	Physical	547mm x 439mm x 196mm 21.5" x 17.3" x 7.7"
OPERATING	Temperature	32-95°F (0-35°C)
CONDITIONS	Humidity	8-80% (non-condensing)
WEIGHT	Net	28.6 lb. (13.0 kg)
	Gross	39.6 lb. (18.0 kg)
WARRANTY		Three-year limited warranty on parts, labor and backlight.

* These are recommendations only. There are variables that may require alterations to these dimensions, such as wall mount depth, non-ViewSonic stand height, etc. Specifications and pricing subject to change without notice. Selections, offers and programs may vary by country; see your ViewSonic representative for complete details. Prices in U.S. dollars.

[Overview](#) | [Features](#) | [Specs](#) | [Accessories](#)



Specifications and pricing subject to change without notice. Selections, offers and programs may vary by country; see your ViewSonic representative for complete details. Prices in U.S. dollars.

EXHIBIT 25



9.2 Million Pixels, TFT Color Monitor

22.2 inch LCD Color Monitor

The Best Professional Ultra-High-Density LCD Color Monitor

**Total Storage
Solution Provider**

ADTX's Ultra-high-density TFT liquid crystal color monitor delivers outstanding visual performance. With a QUXGA-W 3840x2400 high resolution and packing over 9.2 million pixels into its 22.2 inches viewing image area, the ADTX 22.2 TFT monitor displays exceptionally high-quality images and can clearly view even minute images with its 0.1245 mm pixel pitch.

Ultra-high-density QUXGA-W Display

The ultra-high-density display with QUXGA-W (3,840 x 2,400) is four times more than the past UXGA (1,600 x 1,200) that makes it possible to view high-resolution images. As a result, compared with the past UXGA, small images can be viewed in a large scale, image reduction work is greatly decreased, and desired image result is achieved in a very short time.

Wide Viewing Angle Range

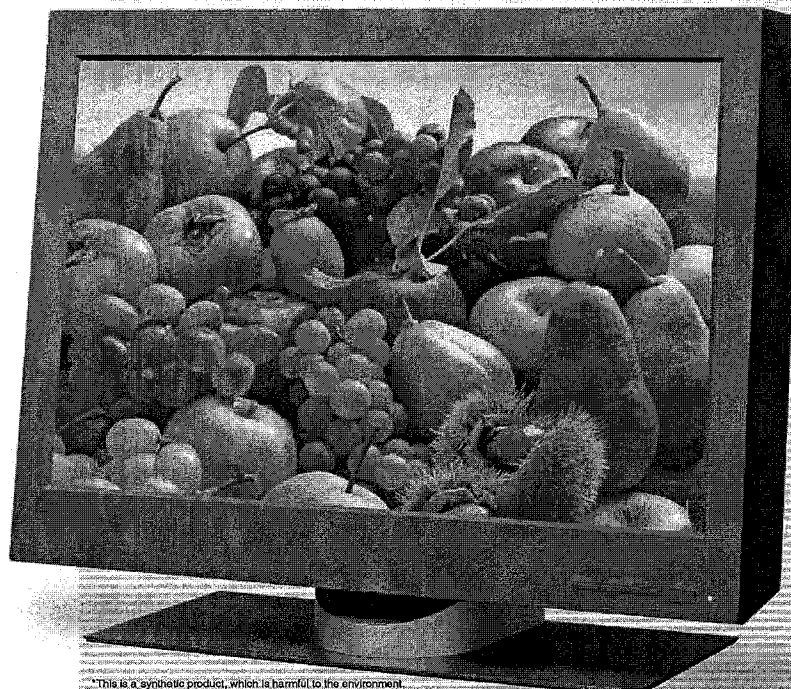
There is a wide view range of horizontal $\pm 85^\circ$ and vertical $\pm 85^\circ$, so the image can be viewed from almost.

Sharp Image Display

In addition to the 16.7 million colors (full-color) and a high-performance contrast ratio of 400:1, a sharp image is displayed, even without any adjustments, through its digital interface (DVI-D).

Wide Application in Various Fields

Applications for this monitor is best for any field that requires extremely high-resolution images -- medicine, product design and development, weather forecasting, publishing and graphic design, banking and finance, digital archiving, satellite mapping and many more.



**For
MAC**

9.2 M pixels

1 Year-Warranty Period

* Warranty is effective from the date of purchase

22.2 inch LCD Color Monitor

Product Specification	
MODEL Name	22.2-Inch TFT High Resolution Color Monitor
MODEL	MD22292C2
Pixel Pitch	0.1245mm(width) x 0.1245mm(height)
Screen Active Area	478.1mm(width) x 298.8mm (height)
Maximum Resolution	3,840 x 2,400
Supported Modes	VGA, SVGA, XGA, SXGA, UXGA, QXGA, QUXGA-W
Maximum	235cd/m ²
Contrast Ratio	400:1
Refresh Rate	13 – 85Hz
Response Speed	Optical Rise Time 25msec / Optical Fall Time
Viewable Angle Range	Horizontal ±85° / Vertical ±85°
No. Of Maximum Display Colors	16.7 Million Colors (Full Color)
Input Connectors	DVI-D
Temperature Range (degree C)	0 – 35(operating) / -20 – 60 (storage)
Humidity [%RH]	8 – 80(Operating/Non-Operating) Max.wet bulb temp. 23.deg.C, No Condensation
Power Consumption	Maximum 150W
Plug&Play	VESA DDC 2B Protocol (Supported with MAC OS 9.x.x)
Physical Size	439(Height) x 547(Width) x 196(Depth) mm
Weight	Approximately12kg
Power Supply	AC100V – 240V, 50/60Hz
Accessories	Video Interface Cables, AC Adaptor, Power Supply Cable (3 pins), Installation CD-ROM, User's Guide, and Warranty Slip

[NOTE:] A special graphic adapter card is needed and is sold separately for this product.

Recommended Graphics Card
ATI RADEON 8500 Mac EDITION
Supported OS
Mac OS 9.xx, Mac OS X
Supported machine Model
Power Mac G4 with one full-size AGP bus

[NOTE:]

1. The product specification contained in this catalog may be changed without prior notice.
2. The ADTX logo mark is a registered trademark of ADTX Systems Co., Ltd.
3. ATI and RADEON are registered trademarks in Canada, the United States, and other countries of ATI Technologies Inc.
4. Mac is a registered trademark in the United States and other Countries of Apple Computer Inc
5. Company name description, business card logo or brand name, and each company name is a registered trademark.
6. This catalog was made in September 2002.
7. This catalog is an English translation from its Japanese version intended for the Japanese market.

The specifications, services, and guarantees for the products described are different from those applicable for use overseas.



Safety Precautions

■ Please read "Safety Precautions" section of the product manual.

Distributor



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Kanagawa-ken, 240-0005, JAPAN
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